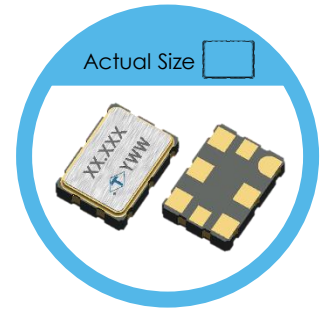


# OD-M Type High Frequency & Ultra Low Noise 7.0 x 5.0 mm Differential Output Crystal Oscillator



**RoHS Compliant**

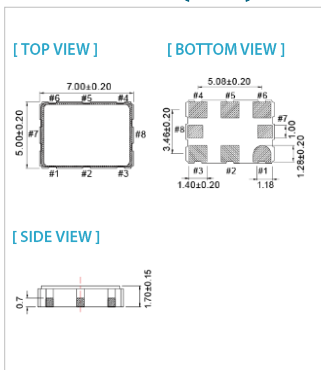
## FEATURES

- Pb-free/RoHS Compliant
- Tri-state Enable / Disable Mode
- Temperature Range: -40 to 85 °C
- Clock Output: LVPECL, LVDS, CML and HCSL
- Output Frequency Support from 15MHz to 2.1GHz
- Low Power Supply Voltage: 3.3, 2.5, and 1.8V Supply Options
- Ultra Low Noise, Phase Jitter < 300fs (Typical: 150fs at 12kHz to 20MHz Frequency Offsets)

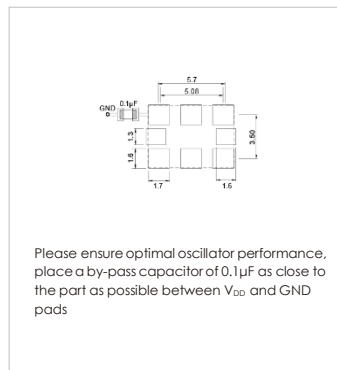
## TYPICAL APPLICATION

- SONET/SDH, Gigabit Ethernet
- Storage Area Networking (SAN)
- SD/HD Video
- FPGA Clock Generation

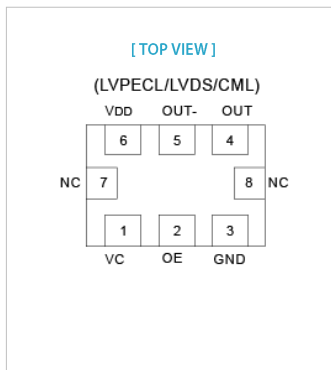
## DIMENSION (mm)



## SOLDER PAD LAYOUT (mm)



## PIN ASSIGNMENTS



## PIN FUNCTION

PIN#	FUNCTION
1	NC
2	OE
3	GND
4	Output
5	Comp. Output
6	V <sub>DD</sub>
7	NC
8	NC

## ELECTRICAL SPECIFICATION

Parameter	LVPECL				Unit	Test Condition
	3.3V		2.5V			
	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V <sub>DD</sub> ) ±10%	V <sub>DD</sub> - 10%	V <sub>DD</sub> + 10%	V <sub>DD</sub> - 10%	V <sub>DD</sub> + 10%	V	
Frequency Range	15	2100	15	2100	MHz	
Standard Frequency	100, 106.25, 125, 156.25, 187.5, 200, 212.5, 266, 300, 312.5, 400				MHz	
Supply Current	110		95		mA	
Output Level	Output High	V <sub>DD</sub> - 1.165	V <sub>DD</sub> - 0.8	V <sub>DD</sub> - 1.165	V <sub>DD</sub> - 0.8	V
	Output Low	V <sub>DD</sub> - 2.0	V <sub>DD</sub> - 1.55	V <sub>DD</sub> - 2.0	V <sub>DD</sub> - 1.55	V
Transition Time (20% - 80%)	Rise Time	0.35		0.35		nSec
	Fall Time	0.35		0.35		nSec
Duty Cycle	45	55	45	55	%	
Startup Time	8				mSec	
Tri-State Mode (Input to Pin 2)	Enable	0.7 x V <sub>DD</sub>		0.7 x V <sub>DD</sub>		V
	Disable	0.3 x V <sub>DD</sub>		0.3 x V <sub>DD</sub>		V
Stand by Current	110		95		mA	
Phase Noise	Typ.	Max.	Typ.	Max.		
At V <sub>DD</sub> =3.3V, f <sub>out</sub> =873.515MHz	1kHz offset	-106		-106		dBc/Hz
	10kHz offset	-115		-115		dBc/Hz
	100kHz offset	-123		-123		dBc/Hz
	1MHz offset	-133		-133		dBc/Hz
	20MHz offset	-150		-150		dBc/Hz
RMS Phase Jitter (Integrated 12 kHz-20 MHz)	150	300	150	300	fs	
Period Jitter	50		50		ps	

**Note: not all combination of options are available. Other specifications may be available upon request.**

Specifications subject to change without notice.

Parameter	LVDS						Unit	Test Condition
	3.3V		2.5V		1.8V			
	Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V <sub>DD</sub> )	2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range	15	2100	15	2100	15	2100	MHz	
Standard Frequency	100, 106.25, 125, 156.25, 187.5, 200, 212.5, 266, 300, 312.5, 400						MHz	
Supply Current		90		80		70	mA	
Output Level	Output High		1.6		1.6		1.6	V
	Output Low	0.9		0.9		0.9		V
Transition Time (20% – 80%)	Rise Time		0.35		0.35		0.35	nSec
	Fall Time		0.35		0.35		0.35	nSec
Duty Cycle		45		45		45		%
Startup Time		8		8		8		mSec
Tri-State Mode (Input to Pin 2)	Enable	0.7 x V <sub>DD</sub>		0.7 x V <sub>DD</sub>		0.7 x V <sub>DD</sub>		V
	Disable		0.3 x V <sub>DD</sub>		0.3 x V <sub>DD</sub>		0.3 x V <sub>DD</sub>	V
Stand by Current		90		80		70		mA
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At V <sub>DD</sub> =3.3V, f <sub>out</sub> =873.515MHz	1kHz offset	-106		-106		-106		dBc/Hz
	10kHz offset	-115		-115		-115		dBc/Hz
	100kHz offset	-123		-123		-123		dBc/Hz
	1MHz offset	-133		-133		-133		dBc/Hz
	10MHz offset	-150		-150		-150		dBc/Hz
RMS Phase Jitter (Integrated 12 kHz~20 MHz)	150	300	150	300	150	300		fs
Period Jitter		50		50		50		ps

Parameter	HCSL						Unit	Test Condition
	3.3V		2.5V		1.8V			
	Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V <sub>DD</sub> )	2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range	15	700	15	700	15	700	MHz	
Supply Current		115		100		94		mA
Output Level	Output High	0.66	1.15	0.66	1.15	0.66	1.15	V
	Output Low	0	0.15	0	0.15	0	0.15	V
Transition Time (20% – 80%)	Rise Time		0.4		0.4		0.4	nSec
	Fall Time		0.4		0.4		0.4	nSec
Duty Cycle		45		45		45		%
Startup Time		8		8		8		mSec
Tri-State Mode (Input to Pin 2)	Enable	0.7 x V <sub>DD</sub>		0.7 x V <sub>DD</sub>		0.7 x V <sub>DD</sub>		V
	Disable		0.3 x V <sub>DD</sub>		0.3 x V <sub>DD</sub>		0.3 x V <sub>DD</sub>	V
Stand by Current		115		100		94		mA
Output Load	50Ω to GND							
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At V <sub>DD</sub> =3.3V, f <sub>out</sub> =873.515MHz	1kHz offset	-87		-87		-87		dBc/Hz
	10kHz offset	-110		-110		-110		dBc/Hz
	100kHz offset	-127		-127		-127		dBc/Hz
	1MHz offset	-138		-138		-138		dBc/Hz
	10MHz offset	-153		-153		-153		dBc/Hz
RMS Phase Jitter (Integrated 12 kHz~20 MHz)	150	300	150	300	150	300		fs
Period Jitter		50		50		50		ps

Parameter	CML						Unit	Test Condition
	3.3V		2.5V		1.8V			
	Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V <sub>DD</sub> )	2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range	15	2100	15	2100	15	2100	MHz	
Standard Frequency	100, 106.25, 125, 156.25, 187.5, 200, 212.5, 266, 300, 312.5, 400						MHz	
Supply Current		90		80		70		mA
Output Level	Output High	V <sub>DD</sub> – 0.085	V <sub>DD</sub>	V <sub>DD</sub> – 0.085	V <sub>DD</sub>	V <sub>DD</sub> – 0.085	V <sub>DD</sub>	V
	Output Low	V <sub>DD</sub> – 0.6	V <sub>DD</sub> – 0.32	V <sub>DD</sub> – 0.6	V <sub>DD</sub> – 0.32	V <sub>DD</sub> – 0.6	V <sub>DD</sub> – 0.32	V
Transition Time (20% – 80%)	Rise Time		0.35		0.35		0.35	nSec
	Fall Time		0.35		0.35		0.35	nSec
Duty Cycle		45		45		45		%
Startup Time		8		8		8		mSec
Tri-State Mode (Input to Pin 2)	Enable	0.7 x V <sub>DD</sub>		0.7 x V <sub>DD</sub>		0.7 x V <sub>DD</sub>		V
	Disable		0.3 x V <sub>DD</sub>		0.3 x V <sub>DD</sub>		0.3 x V <sub>DD</sub>	V
Stand by Current		90		80		70		mA
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At V <sub>DD</sub> =3.3V, f <sub>out</sub> =873.515MHz	1kHz offset	-107		-107		-107		dBc/Hz
	10kHz offset	-117		-117		-117		dBc/Hz
	100kHz offset	-125		-125		-125		dBc/Hz
	1MHz offset	-135		-135		-135		dBc/Hz
	10MHz offset	-150		-150		-150		dBc/Hz
RMS Phase Jitter (Integrated 12 kHz~20 MHz)	150	300	150	300	150	300		fs
Period Jitter		50		50		50		ps

**Note: not all combination of options are available. Other specifications may be available upon request.**

Specifications subject to change without notice.

## FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C)	ppm			
	±20	±25	±30	±50
-20 ~ +70	△	○	○	○
-40 ~ +85	×	△	○	○

○: Available △:Conditional ×: Not Available  
 Inclusive of calibration @ 25°C ,operating temperature range,input  
 Voltage variation,load variation,aging (1<sup>st</sup> year),shock,and vibration

**Note: not all combination of options are available. Other specifications may be available upon request.**

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